The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A carry chain in a logic array block having a set of logic elements, the carry chain comprising:

a first path connecting a first series of logic elements in the logic array block,

wherein the logic elements in the first series is a subset of the set of logic elements in the logic array block; **[[and]]**

a second path connecting a second series of logic elements in the logic array block,

wherein one or more of the logic elements in the second series are not in the first series; **and**

a multiplexer having a first input and a second input,

wherein when the first input is selected, a carry signal is propagated through the first series of logic elements, and

wherein when the second input is selected, the carry signal is propagated through the second series of logic elements.

2. (original) The carry chain of claim 1, wherein the logic elements in the first series are a subset of the logic elements in the second series.

3. (cancelled)

4. (currently amended) The carry chain of claim **[[3]] 1**, wherein the multiplexer is located in a middle portion of the logic array block.

5. (currently amended) The carry chain of claim **[[3]] 1**, wherein the multiplexer is located at a bottom portion of the logic array block.

6. (currently amended) The carry chain of claim 2, further comprising:

a multiplexer located at a top portion of the logic array block having a first input and a second input,

wherein when the first input is selected, the carry signal is propagated through a first series of logic elements of a preceding logic array block, and

wherein when the second input is selected, the carry signal is propagated through a second series of logic elements of a preceding logic array block.

7. (original) The carry chain of claim 1, further comprising:

a first multiplexer configured to bypass a first portion of the carry chain, wherein the logic elements in the first series are located in the first portion; and

a second multiplexer configured to bypass a second portion of the carry chain, wherein the logic elements in the second series are located in the second portion.

8. (original) The carry chain of claim 7,

wherein the first multiplexer includes:

a first input connected to a beginning of the first series,

a second input connected to an end of the first series,

an output connected to a beginning of the second series, and

wherein the second multiplexer includes:

a first input connected to the end of the first series, and

a second input connected to an end of the second series.

9. (original) The carry circuit of claim 1, further comprising:

a redundancy circuit connected to the first path and the second path, wherein the redundancy circuit is configured to skip a logic array block in a column of logic array blocks.

10. (original) The carry circuit of claim 9, wherein the redundancy circuit comprises:

a multiplexer having:

a first input connected to an output of a carry chain from a preceding logic array block in a preceding row,

a second input connected to the first input of a multiplexer in a redundancy circuit of the preceding logic array block in the preceding row, and

an output connected to the first path.

11. (original) The carry circuit of claim 1, further comprising:

a carry select circuit connected to the first path and the second path, wherein the carry select circuit is configured to provide a first pre-computed value and a second pre-computed value for a set of logic elements.

12. (original) The carry circuit of claim 11, wherein the carry select circuit comprises:

a first multiplexer having:

a first input connected to the first series of logic elements, wherein the first input provides the first pre-computed value for the first series of logic elements,

a second input connected to the first series of logic elements, wherein the second input provides the second pre-computed value for the first series of logic elements,

an output connected to the second series of logic elements,

wherein the first multiplexer receives a carry select signal from an input to the first path, and

a second multiplexer having:

a first input connected to the second series of logic elements, wherein the first input provides the first pre-computed value for the second series of logic elements,

a second input connected to the second series of logic elements, wherein the second input provides the second pre-computed value for the second series of logic elements, and

wherein the second multiplexer receives a carry select signal from the output of the first multiplexer.

13. (original) The carry chain of claim 1, further comprising:

a first carry chain defined by the first path;

at least a second carry chain defined by the second path,

wherein each of the logic elements in the second series are not in the first series.

14. (original) The carry chain of claim 1, further comprising:

one or more metal layer option regions disposed within the first and second paths,

wherein each metal layer option region includes a first layout and a second layout, and

wherein a first region of the logic array block is bypass-able when the metal layer option regions are formed in accordance with the first layout, and

wherein a second region of the logic array block is bypass-able when the metal layer option regions are formed in accordance with the second layout.

15. (original) The carry chain of claim 1, further comprising:

a first column of logic array blocks, each logic array block in the first column having a carry chain with the first path located in a top portion of the carry chain; and

a second column of logic array blocks adjacent to the first column, each logic array block in the second column having a carry chain with the first path located in a bottom portion of the carry chain, wherein the second column is adjacent to the first column.

16. (original) A programmable logic device including the carry chain of claim 1.

17. (original) A digital system comprising a programmable logic device including the carry chain of claim 1.

18. (currently amended) A programmable logic device comprising:

an array of logic elements grouped into a plurality of logic array blocks; and

a carry circuit disposed within a logic array block, the carry circuit configured to operate in a first mode and a second mode,

wherein when the carry circuit operates in [[a]] the first mode, a carry signal is propagated through a first series of logic elements within the logic array block, and

wherein when the carry circuit operates in [[a]] the second mode, a carry signal is propagated through a second series of logic elements within the logic array block,

the first series of logic elements being a subset of the second series of logic elements.

19. (original) The programmable logic device of claim 18, wherein the carry chain further comprises:

a multiplexer having a first input and a second input,

wherein when the first input is selected, the carry signal is propagated through the first series of logic elements, and

wherein when the second input is selected, the carry signal is propagated through the second series of logic elements.

20. (original) The programmable logic device of claim 18, wherein the carry chain further comprises:

a first multiplexer configured to bypass a first portion of the carry chain, wherein the logic elements in the first series are located in the first portion; and

a second multiplexer configured to bypass a second portion of the carry chain, wherein one or more of the logic elements in the second series are located in the second portion.

21. (original) The programmable logic device of claim 18, further comprising:

a redundancy circuit connected to the carry chain, wherein the redundancy circuit is configured to skip a logic array block in a column of logic array blocks.

22. (original) The programmable logic device of claim 21, wherein the redundancy circuit comprises:

a multiplexer having:

a first input connected to an output of a carry chain from a preceding logic array block in a preceding row,

a second input connected to the first input of a multiplexer in a redundancy circuit of the preceding logic array block in the preceding row, and

an output connected to the carry chain.

23. (original) The programmable logic device of claim 18, further comprising:

a carry select circuit connected to the carry chain, wherein the carry select circuit is configured to provide a first pre-computed value and a second pre-computed value for a set of logic elements.

24. (original) The programmable logic device of claim 18, further comprising:

one or more metal layer option regions disposed within the carry chain,

wherein each metal layer option region includes a first layout and a second layout, and

wherein a first region of the logic array block is bypass-able when the metal layer option regions are formed in accordance with the first layout, and

wherein a second region of the logic array block is bypass-able when the metal layer option regions are formed in accordance with the second layout.

25. (original) The programmable logic device of claim 18, further comprising:

a first column of logic array blocks, each logic array block in the first column having a carry chain with the first series of logic elements located in a top portion of the carry chain; and

a second column of logic array blocks adjacent to the first column, each logic array block in the second column having a carry chain with the first series of logic elements located in a bottom portion of the carry chain, wherein the second column is adjacent to the first column.

26. (original) A digital system comprising the programmable logic device of claim 18.

27. (original) A method of forming a carry chain in a logic array block having a set of logic elements, the method comprising:

forming a first path connecting a first series of logic elements in the logic array block,

wherein the logic elements in the first series is a subset of the set of logic elements in the logic array block; and

forming a second path connecting a second series of logic elements in the logic array block,

wherein one or more of the logic elements in the second series are not in the first series.